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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,440	09/27/2001	Akira Yamaguchi	2102475-991160	5355

26379 7590 08/29/2002

GARY CARY WARE & FREIDENRICH LLP
1755 EMBARCADERO ROAD
PALO ALTO, CA 94303-3340

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

#7

Office Action Summary	Application No.	Applicant(s)	
	09/966,440	YAMAGUCHI ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133)
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed matter in claim 10 where the first intermediate layer is the uppermost layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 8 does not distinctly point out the meaning of the first intermediate layer is on said lowermost layer side compared with said second intermediate layer. Examiner is unable to identify if the Applicant's first intermediate layer is directly on the lowermost layer or is the first intermediate layer any layer above the lowermost layer with a second intermediate layer disposed there in.

3. Claims 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 10 claims intermediate layers between the first intermediate layer and the uppermost layer, but the claim later teaches the uppermost layer to be the first intermediate layer. It is unclear to the examiner to see the Applicant's invention.

Claim Rejections - 35 USC § 102

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,262,487 Igarashi et al. (insofar as to understand the claims based off of the 35 U.S.C. 112, second paragraph rejection).

4. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 21 #10); a lowermost layer, (Figure 21 #601), nearest to said semiconductor substrate, (Figure 21 #10); an uppermost layer, (Figure 21 #605), farthest from said semiconductor

substrate, (Figure 21 #10); and intermediate layers, (Figure 21 #603 & 604), arranged between said lowermost layer, (Figure 21 #601), and said uppermost layer, (Figure 21 #605); wherein when one of said intermediate layers, (Figure 21 #603 & 604), is set as a first intermediate layer, (Figure 21 #604), and the other one of said intermediate layers, (Figure 21 #603 & 604), is set as a second intermediate layer, (Figure 21 #603), said first intermediate layer, (Figure 21 #604), is on said lowermost layer side, (Figure 21 #601), compared with said second intermediate layer, (Figure 21 #603), and said first intermediate layer, (Figure 21 #604), is thicker than said second intermediate layer, (Figure 21 #603).

5. Referring to claim 2, a semiconductor device, wherein a wiring pitch of said first intermediate layer, (Figure 21 #604), is wider than a wiring pitch of said second intermediate layer, (Figure 21 #603).

6. Referring to claim 6, a semiconductor device, wherein said first intermediate layer, (Figure 21 #604), is substantially as thick as said uppermost layer, (Figure 21 #605).

7. Referring to claim 7, a semiconductor device, wherein said second intermediate layer, (Figure 21 #603), is substantially as thick as said lowermost layer, (Figure 21 #601).

8. Referring to claim 8, a semiconductor device, wherein all of said uppermost layer, (Figure 21 #605), said lowermost layer, (Figure 21 #601), and said intermediate layers, (Figure 21 #603 & 604), are metal layers, (Col. 12 Lines 22-26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10, 12-14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,262,487 Igarashi et al., (insofar as to understand the claims based off of the 35 U.S.C. 112, second paragraph rejection).

9. Referring to claim 9, a semiconductor device comprising: a semiconductor substrate, (Igarashi et al. Figure 21 #10); an IP core area, (Igarashi et al. Col. 1 Lines 8-10), on said semiconductor substrate, (Igarashi et al. Figure 21 #10); a peripheral area on said semiconductor substrate, (Igarashi et al. Figure 21 #10), except for said IP core area, (Igarashi et al. Col. 1 Lines 8-10); a lowermost layer, (Igarashi et al. Figure 21 #601), nearest to said semiconductor substrate, (Igarashi et al. Figure 21 #10); an uppermost layer, (Igarashi et al. Figure 21 #605), farthest from said semiconductor substrate, (Igarashi et al. Figure 21 #10); and intermediate substrates arranged between said lowermost layer, (Igarashi et al. Figure 21 #601), and said uppermost layer, (Igarashi et al. Figure 21 #605); wherein when one of said intermediate layers, (Igarashi et al. Figure 21 #603 & 604), is set as a first intermediate layer, (Igarashi et al. Figure 21 #604), and the other one of said intermediate layers, (Igarashi et al. Figure 21 #603 & 604), is set as a second intermediate layer, (Igarashi et al. Figure 21 #603), said first intermediate layer, (Igarashi et al. Figure 21 #604), is on said lowermost layer, (Igarashi et al. Figure 21 #601), side

compared with said second intermediate layer, (Igarashi et al. Figure 21 #603), and said first intermediate layer, (Igarashi et al. Figure 21 #604), is thicker than said second intermediate layer, (Igarashi et al. Figure 21 #603).

Igarashi et al. teaches all of the claimed matter in claim 9 except for the IP Core, but Igarashi et al. teaches an integrated circuit. Implementing these teachings from an IC to an IP would have been an obvious design choice since both designs are used for information storage.

10. Referring to claim 10, a semiconductor device, (insofar as to understand the claims based off of the 35 U.S.C. 112, second paragraph rejection), wherein said uppermost layer, (Igarashi et al. Figure 21 #605), and all the intermediate layers, (Igarashi et al. Figure 21 #603 & 604), between said first intermediate layer, (Igarashi et al. Figure 21 #604), and said uppermost layer, (Igarashi et al. Figure 21 #605), are formed only in said peripheral area, and said first intermediate layer, (Igarashi et al. Figure 21 #604), is an uppermost layer, (Igarashi et al. Figure 21 #605), farthest to said semiconductor substrate, (Igarashi et al. Figure 21 #10), in said IP core area, (Igarashi et al. Col. 1 Lines 8-10).

Igarashi et al. teaches all of the claimed matter in claim 10 except for the IP Core, but Igarashi et al. teaches an integrated circuit. Implementing these teachings from an IC to an IP would have been an obvious design choice since both designs are used for information storage.

11. Referring to claim 12, a semiconductor device, wherein a wiring pitch of said first intermediate layer, (Figure 21 #604), is wider than a wiring pitch of said second intermediate layer, (Figure 21 #603).

12. Referring to claim 13, a semiconductor device, wherein said first intermediate layer, (Figure 21 #604), is substantially as thick as said uppermost layer, (Figure 21 #605).

13. Referring to claim 14, a semiconductor device, wherein said second intermediate layer, (Figure 21 #603), is substantially as thick as said lowermost layer, (Figure 21 #601).

14. Referring to claim 17, a semiconductor device, wherein all of said uppermost layer, (Figure 21 #605), said lowermost layer, (Figure 21 #601), and said intermediate layers, (Figure 21 #603 & 604), are metal layers, (Col. 12 Lines 22-26).

Claim Rejections - 35 USC § 103

Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,262,487 Igarashi et al. in view of U.S. Patent No. 6,246,112 Ballo et al., (insofar as to understand the claims based off of the 35 U.S.C. 112, second paragraph rejection).

15. Referring to claim 3, a semiconductor device, wherein said first intermediate layer, (Igarashi et al. Figure 21 #604), is a layer on which a power source line, (Ball et al. Figure 2 #22), is formed.

Igarashi et al. teaches all of the claimed matter in claim 3 except for the first intermediate layer being a layer that contains a power source line. Igarashi et al. does not identify the intermediate layers as being a source or a signal line, but Ball et al. does. It would have been obvious to one skilled in the art to combine the teachings of Igarashi et al. with the teachings of Ball et al. because it is well known that intermediate layers can be source lines and it is also well known to one skilled in the art that integrated circuits need a power source.

16. Referring to claim 11, a semiconductor device, wherein said first intermediate layer, (Igarashi et al. Figure 21 #604), is a layer on which a core power source line, (Ball et al. Figure 2 #22), is formed in said IP core area, (Igarashi et al. Col. 1 Lines 8-10 see ** below).

Igarashi et al. teaches all of the claimed matter in claim 3 except for the first intermediate layer being a layer that contains a power source line. Igarashi et al. does not identify the intermediate layers as being a source or a signal line, but Ball et al. does. It would have been obvious to one skilled in the art to combine the teachings of Igarashi et al. with the teachings of Ball et al. because it is well known that intermediate layers can be source lines and it is also well known to one skilled in the art that integrated circuits need a power source.

** Igarashi et al. teaches all of the claimed matter in claim 9 except for the IP Core, but Igarashi et al. teaches an integrated circuit. Implementing these teachings from an IC to an IP would have been an obvious design choice since both designs are used for information storage.

Allowable Subject Matter

17. Claims 4-5 and 15-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and claims 4-5 and 15-16 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
August 25, 2002